

JEDEC STANDARD

Definition of the SSTUA32S865 and SSTUA32D865 28-bit 1:2 Registered Buffer with Parity for DDR2 RDIMM Applications

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DEFINITION OF THE SSTUA32S865 AND SSTUA32D865 28-BIT 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-05-127 and JCB-07-07, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32S865 and SSTUA32D865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications.

The SSTUA32S865 and SSTUA32D865 are identical in functionality to the SSTU32865 but specify tighter timing characteristics and a higher application frequency of up to 410MHz.

SSTU32S865 denotes a single-die implementation, SSTU32D865 denotes a dual-die implementation.

The purpose is to provide a standard for the SSTUA32S865 and SSTUA32D865 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUA32S865 and SSTUA32D865 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device standard

2.1 Description

This 28-bit 1:2 registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTUA32S865 and SSTUA32D865 operate from a differential clock (CK and \overline{CK}). Data are registered at the crossing of CK going high, and \overline{CK} going low.

The device supports low-power standby operation. When the reset input (\overline{RESET}) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when \overline{RESET} is low all registers are reset, and all outputs except \overline{PTYERR} are forced low. The LVCMOS \overline{RESET} input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, \overline{RESET} must be held in the low state during power up.

2 Device standard (cont'd)

2.1 Description (cont'd)

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTUA32S865 and SSTUA32D865 must ensure that the outputs will remain low, thus ensuring no glitches on the output. If the data inputs are not held low, then $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ must be held high, DODT0 and DODT1, DCKE0, and DCKE1 must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{\text{RESET}}$.

The device monitors both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ are high. If either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ input is low, the Qn outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and will force the Qn outputs low and the $\overline{\text{PTYERR}}$ output high. If the DCS-control functionality is not desired, then the CSGateEnable input can be hardwired to ground, in which case, the setup-time requirement for DCS would be the same as for the other D data inputs.

The SSTUA32S865 and SSTUA32D865 include a parity checking function. The SSTUA32S865 and SSTUA32D865 accept a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the D-inputs (with either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ active) and indicates whether a parity error has occurred on its open-drain $\overline{\text{PTYERR}}$ pin (active LOW).

The parity error output $\overline{\text{PTYERR}}$ will be reset to high by $\overline{\text{RESET}}$ transitioning low and will not be decoded until after $\overline{\text{RESET}}$ goes high and $\overline{\text{DCS0}}$ and/or $\overline{\text{DCS1}}$ are asserted low. CSGateEN does not affect $\overline{\text{PTYERR}}$ operation.

Package options include 160-ball Thin Profile Fine Pitch BGA (TFBGA) (12×18 array, 9.0×13.0 mm body size, 0.65 mm pitch, MO-246, Issue A).

2.2 160-ball TFBGA (MO-246A)

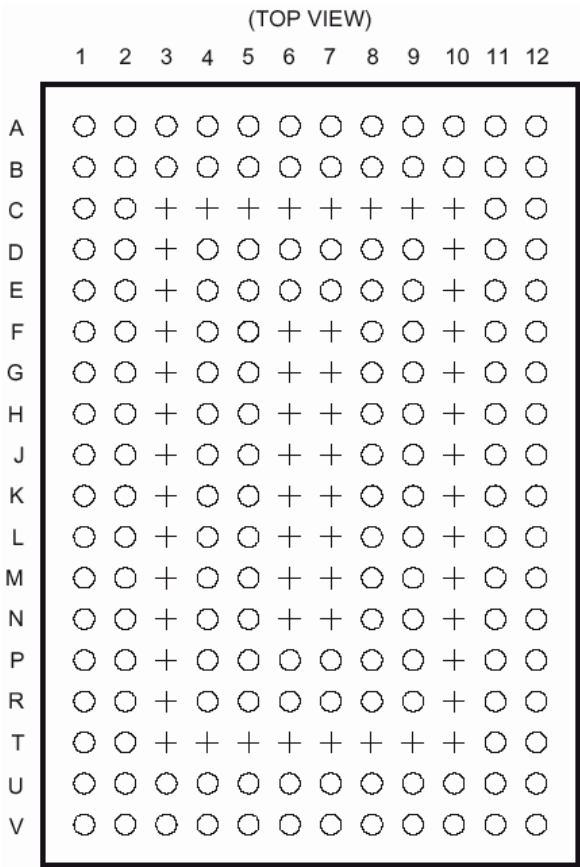


Figure 1 — Pinout configuration

2.3 Pinout top view for 160-ball TFBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	NC	PARIN	NC	NC	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	NC	NC	NC	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VDDL	GND	NC	NC	GND	GND		Q20B	Q20A
E	D7	D8		VDDL	GND	VDDL	VDDR	GND	GND		Q16B	Q16A
F	D11	D9		VDDL	GND			VDDR	VDDR		Q1B	Q1A
G	D18	D12		VDDL	GND			VDDR	VDDR		Q2B	Q2A
H	CSGate EN	D15		VDDL	GND			GND	GND		Q5B	Q5A
J	CK	DCS0		GND	GND			VDDR	VDDR		QCS0B	QCS0A
K	CK	DCS1		VDDL	VDDL			GND	GND		QCS1B	QCS1A
L	RESET	D14		GND	GND			VDDR	VDDR		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VDDL	VDDL			VDDR	VDDR		Q9B	Q9A
P	D19	D21		GND	VDDL	VDDL	VDDR	VDDR	GND		Q11B	Q11A
R	D13	D20		GND	VDDL	VDDL	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14A
U	DCKE0	DCKE1	MCL	PTYERR	MCH	Q3B	Q12B	Q7B	Q4B	Q13B	Q0B	Q8B
V	VREF	MCL	MCL	NC	MCH	Q3A	Q12A	Q7A	Q4A	Q13A	Q0A	Q8A

An empty cell indicates no ball is populated at that gridpoint. NC denotes a no-connect (ball present but not connected to the die). MCL denotes a pin that Must be Connected LOW. MCH denotes a pin that Must be Connected HIGH.

Figure 2 — Pinout top view for 160-ball TFBGA (12 × 18 grid)

2.4 Terminal functions

Table 1 — Terminal functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE0, DCKE1, DODT0, DODT1	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select gated inputs	D0 ... D21	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs	$\overline{DCS0}$, $\overline{DCS1}$	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes and parity checking, and as such at least one will be low when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGateEN high) when at least one Chip Select input is LOW.
Re-driven outputs	Q0A...Q21A, Q0B ... Q21B, $\overline{QCS0}$ -1A,B, QCKE0-1A,B, QODT0-1A,B	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Parity input	PARIN	SSTL_18	Parity input for the D0 ... D21 inputs; arrives one clock cycle after the corresponding data input.
Parity error output	\overline{PTYERR}	Open drain	When LOW, this output indicates that a parity error was identified associated with a valid address and/or command input. \overline{PTYERR} will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition).
Program inputs	CSGateEN	1.8 V LVCMOS	Chip Select Gate Enable. When HIGH, the D0..D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0...D21 inputs will be latched and redriven on every rising edge of the clock.
Clock inputs	CK, \overline{CK}	SSTL_18	Differential controller clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs	MCL, MCH		Must be connected to a logic LOW or HIGH.
	\overline{RESET}	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. \overline{RESET} also resets the \overline{PTYERR} signal.
	VREF	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.

2 Device standard (cont'd)**2.5 Function table****Table 2 — Function table (each flip flop)**

Inputs							Outputs			
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CSGate Enable	CK	$\overline{\text{CK}}$	Dn, DODTn, DCKEn	Qn	$\overline{\text{QCS0}}$	$\overline{\text{QCS1}}$	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q ₀	Q ₀	Q ₀	Q ₀
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q ₀	Q ₀	Q ₀	Q ₀
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q ₀	Q ₀	Q ₀	Q ₀
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q ₀	Q ₀	Q ₀	Q ₀
H	H	H	H	↑	↓	L	Q ₀	H	H	L
H	H	H	H	↑	↓	H	Q ₀	H	H	H
H	H	H	H	L or H	L or H	X	Q ₀	Q ₀	Q ₀	Q ₀
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

2 Device standard (cont'd)**2.5 Function table (cont'd)****Table 3 — Parity and standby function table**

Inputs							Output
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CK	$\overline{\text{CK}}$	Σ of inputs = H (D0-D21)	PARIN*	$\overline{\text{PTYERR}}$ **
H	L	H	↑	↓	Even	L	H
H	L	H	↑	↓	Odd	L	L
H	L	H	↑	↓	Even	H	L
H	L	H	↑	↓	Odd	H	H
H	H	L	↑	↓	Even	L	H
H	H	L	↑	↓	Odd	L	L
H	H	L	↑	↓	Even	H	L
H	H	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$\overline{\text{PTYERR}}_0$ §
H	X	X	L or H	L or H	X	X	$\overline{\text{PTYERR}}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

* PARIN arrives one clock cycle after the data to which it applies. All D inputs must be driven to a known state for parity to be calculated correctly.

** This transition assumes $\overline{\text{PTYERR}}$ is high at the crossing of CK going high and $\overline{\text{CK}}$ going low. If $\overline{\text{PTYERR}}$ is low, it stays latched low for two clock cycles or until $\overline{\text{RESET}}$ is driven low. CSGateEN is “don’t care” for $\overline{\text{PTYERR}}$.

§ If $\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$, and CSGEN are driven high, the device is placed in low-power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the $\overline{\text{PTYERR}}$ output is driven low, it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low.

2 Device standard (cont'd)
2.6 Logic diagram

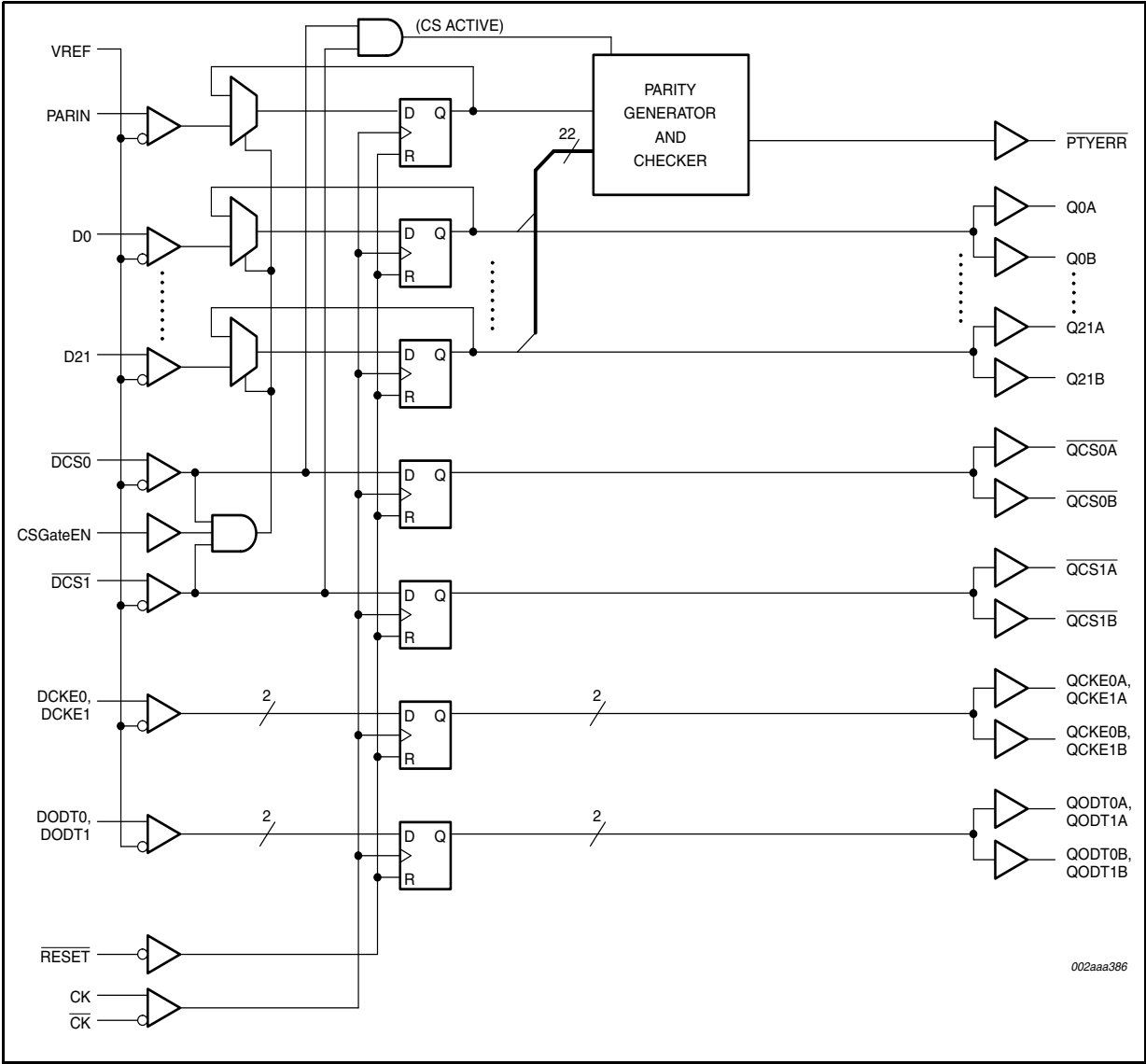


Figure 3 — Logic diagram (positive logic)

2 Device standard (cont'd)

2.7 Register timing

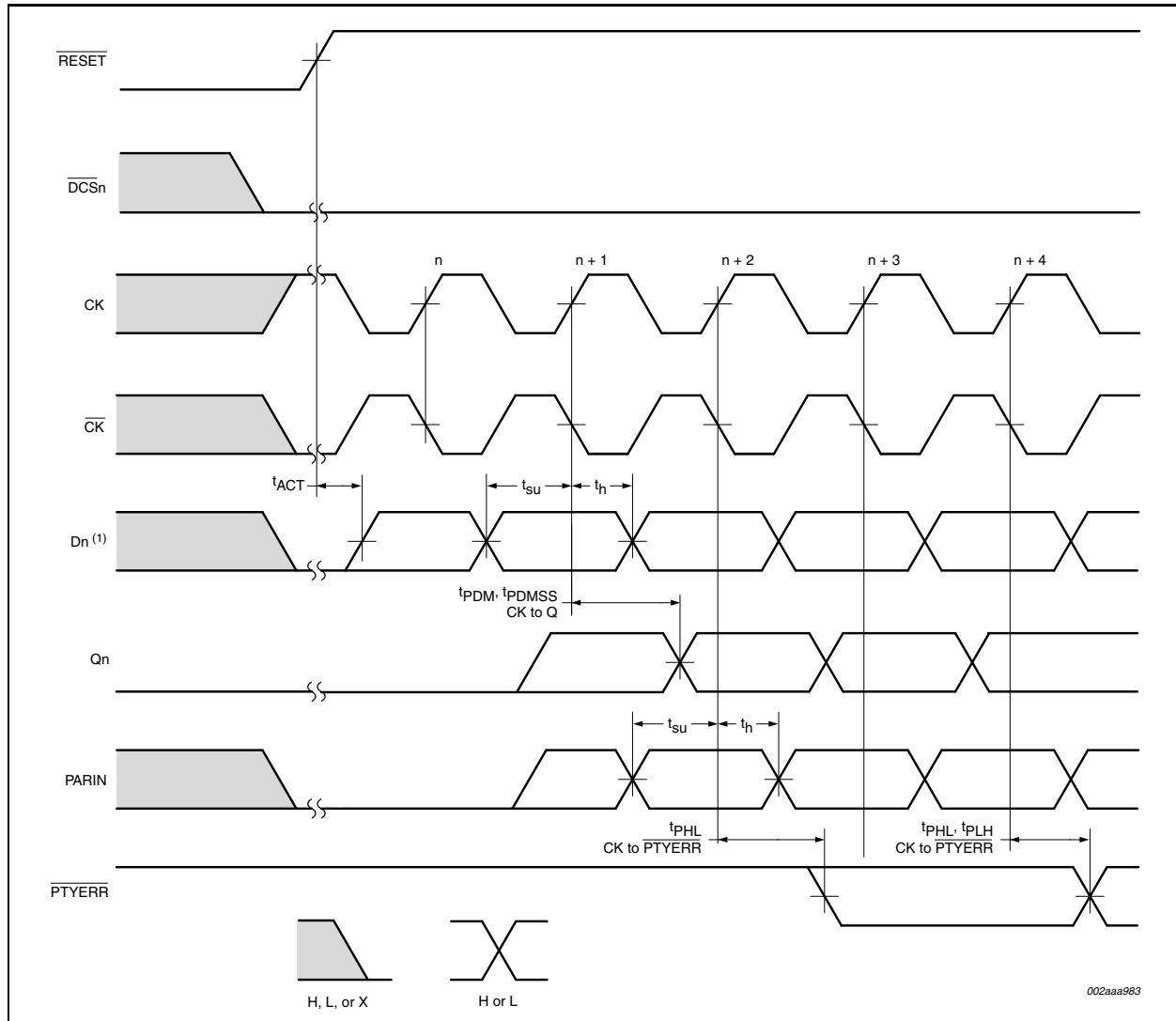


Figure 4 — $\overline{\text{RESET}}$ switches from L to H

(1) After $\overline{\text{RESET}}$ is switched from LOW to HIGH, if $\overline{\text{DCS}}_0$ or $\overline{\text{DCS}}_1$ are held Low than all data and PAR_{IN} input signals must be held Low for a minimum time of t_{ACT} (max.) to avoid false error. If $\overline{\text{DCS}}_0$ or $\overline{\text{DCS}}_1$ are held high than all data and PAR_{IN} input signals must be held at valid logic levels for a minimum time of t_{ACT} (max.) to avoid false error.

2 Device standard (cont'd)

2.7 Register timing (cont'd)

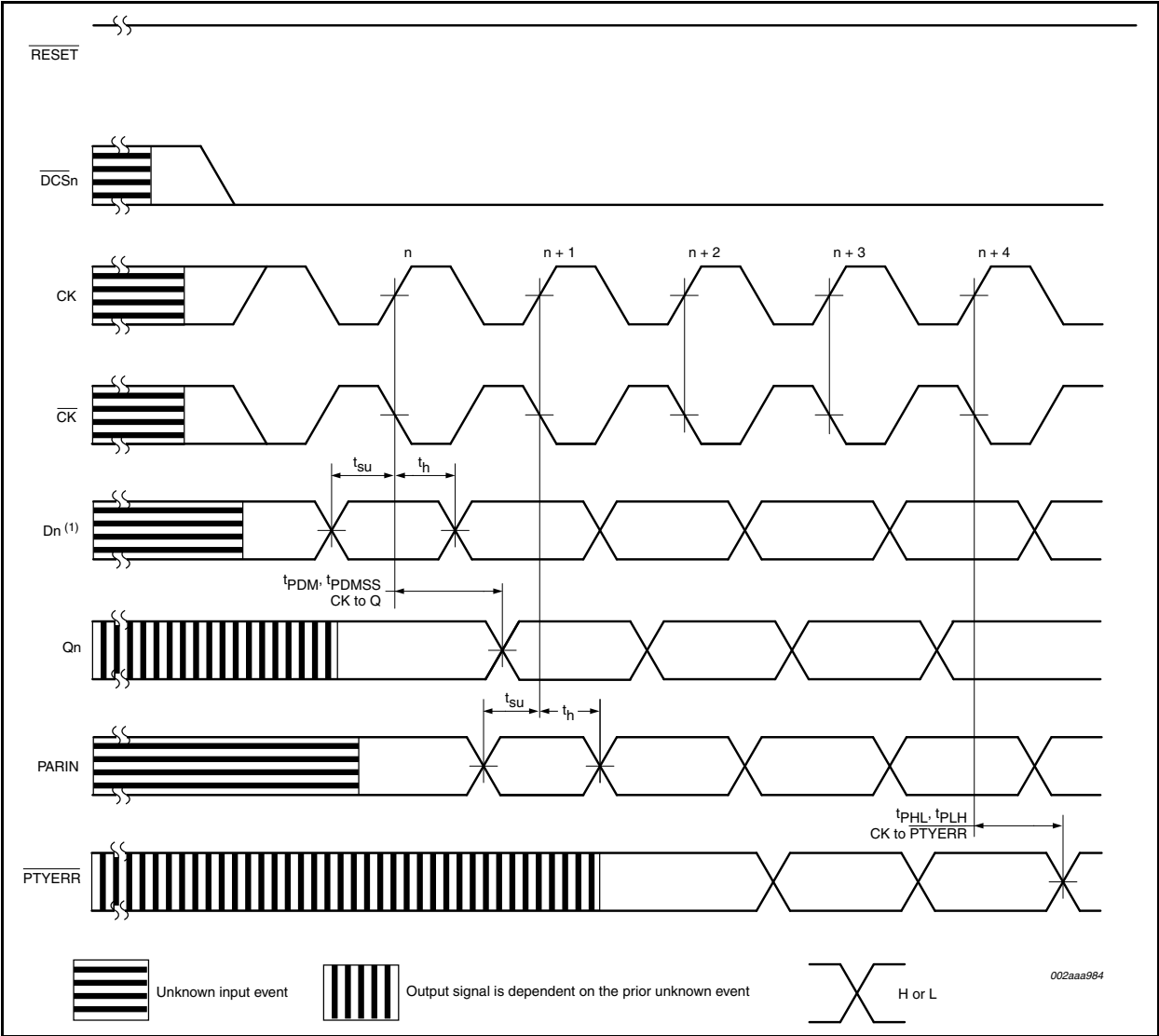
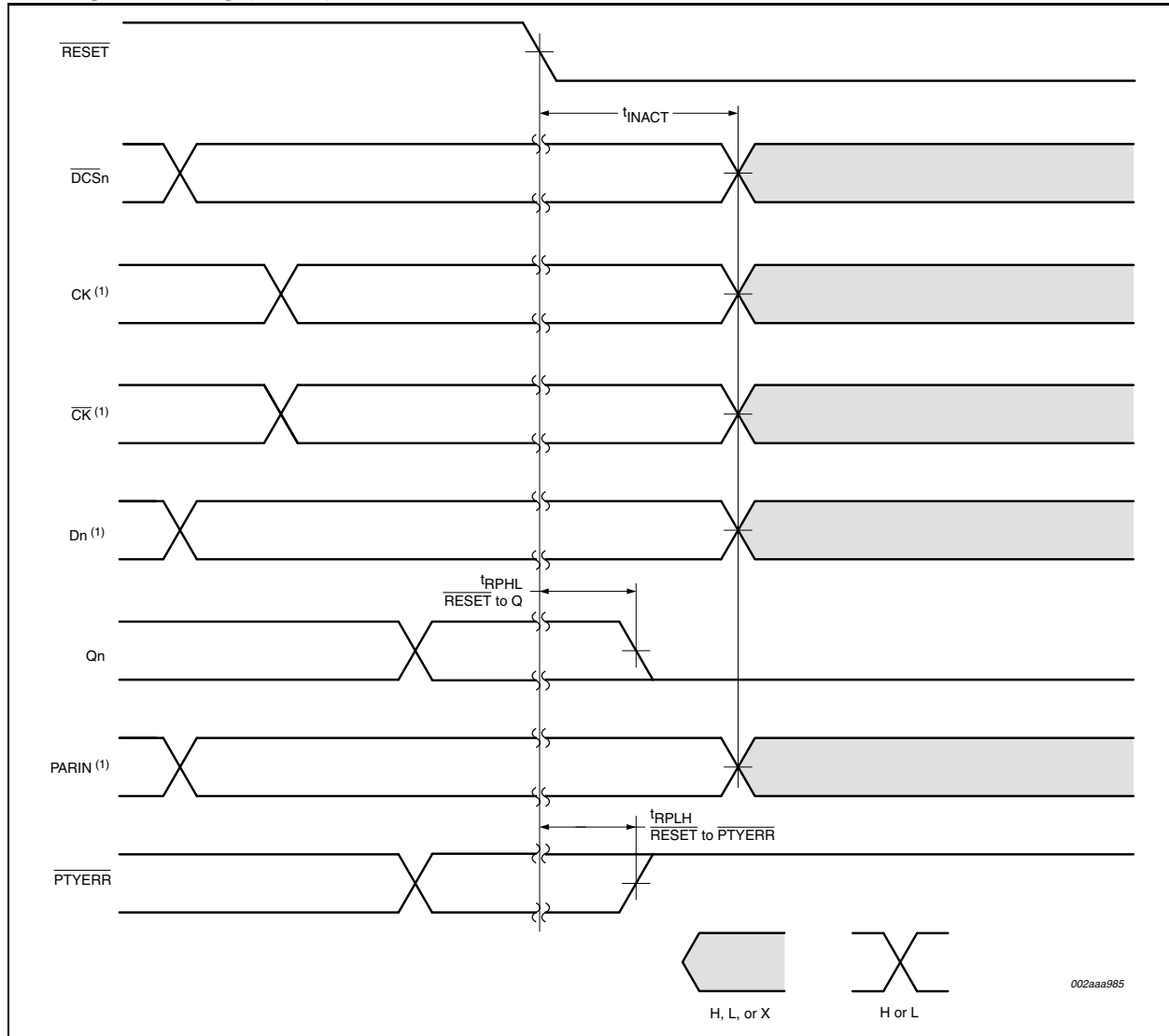


Figure 5 — RESET being held HIGH

2 Device standard (cont'd)

2.7 Register timing (cont'd)

Figure 6 — $\overline{\text{RESET}}$ switches from H to L

(1) After $\overline{\text{RESET}}$ is switched from HIGH to LOW, all data and clock input signals must be set and held at valid logic levels (not floating) for a minimum time of t_{INACT} (max.).

2 Device standard (cont'd)

2.7 Register timing (cont'd)

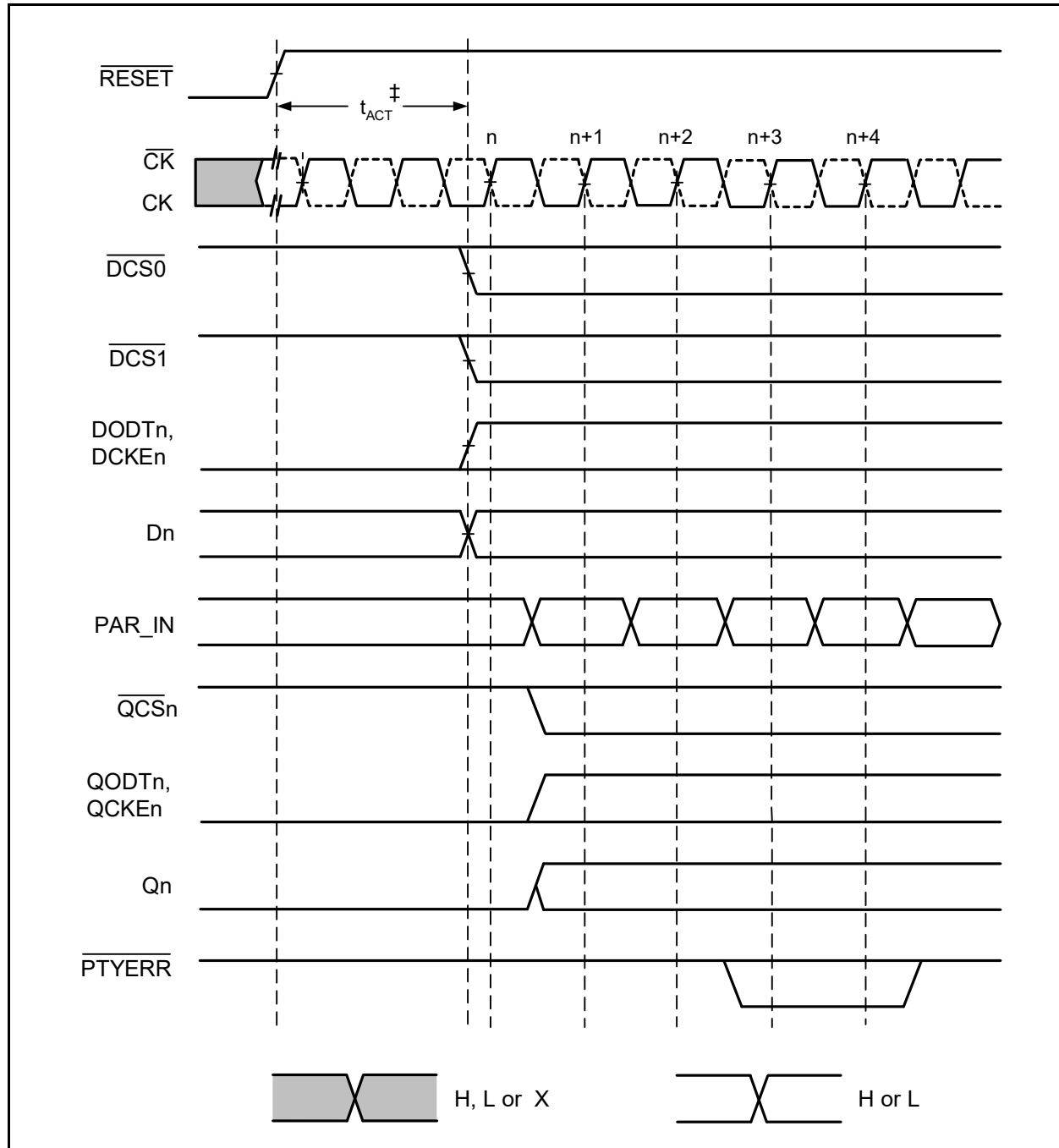


Figure 7 — Timing diagram during start-up when data inputs are Low or High ($\overline{\text{RESET}}$ switches from L to H)

‡

After $\overline{\text{RESET}}$ is switched from low to high, $\overline{\text{DCS0}}$ and $\overline{\text{DSC1}}$ must be held HIGH, DODT0 , DODT1 , DCKE0 and DCKE1 must be held LOW, and all other inputs must remain stable either LOW or HIGH (not floating) for a minimum time of t_{ACT} max.

Figure 9 — Parity logic diagram

2 Device standard (cont'd)**2.9 Absolute maximum ratings****Table 4 — Absolute maximum ratings over operating free-air temperature range (see Note 1)**

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		-0.5	+2.5	V
V_I	Receiver input voltage	(see Note 2)	-0.5	+2.5	V
V_O	Driver output voltage	(see Note 2)	-0.5	$V_{DD} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	-	-50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	-	± 50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	-	± 50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		-	± 100	mA
T_{stg}	Storage temperature		-65	+150	°C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2 Device standard (cont'd)**2.10 Recommended operating conditions****Table 5 — Recommended operating conditions (see Note)**

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DD}	Supply voltage		1.7	-	1.9	V
V_{REF}	Reference voltage		$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{TT}	Termination voltage		$V_{REF} - 40 \text{ mV}$	V_{REF}	$V_{REF} + 40 \text{ mV}$	V
V_I	Input voltage		0	-	V_{DD}	V
V_{IH}	AC HIGH-level input voltage	Data inputs	$V_{REF} + 250 \text{ mV}$	-	-	V
V_{IL}	AC LOW-level input voltage	Data inputs	-	-	$V_{REF} - 250 \text{ mV}$	V
V_{IH}	DC HIGH-level input voltage	Data inputs	$V_{REF} + 125 \text{ mV}$	-	-	V
V_{IL}	DC LOW-level input voltage	Data inputs	-	-	$V_{REF} - 125 \text{ mV}$	V
V_{IH}	HIGH-level input voltage	\overline{RESET} , CSGateEN	$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.35 \times V_{DD}$	V
V_{ICR}	Common-mode input voltage range	CK, \overline{CK}	0.675	-	1.125	V
V_{ID}	Differential input voltage	CK, \overline{CK}	600	-	-	mV
I_{OH}	HIGH-level output current		-	-	-8	mA
I_{OL}	LOW-level output current		-	-	8	mA
I_{ERROL}	\overline{PTYERR} LOW-level output current		25	-	-	mA
T_{amb}	Operating ambient temperature in free-air		0	-	+70	°C

NOTE The \overline{RESET} input of the device must be held at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless \overline{RESET} is LOW.

2.11 DC specifications

Table 6 — Electrical characteristics over recommended operating free-air temperature range

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{OH}	Output HIGH voltage	I _{OH} = −6 mA; V _{DD} = 1.7 V	1.2	-	-	V
V _{OL}	Output LOW voltage	I _{OL} = 6 mA; V _{DD} = 1.7 V	-	-	0.5	V
V _{ERROL}	PTYERR output LOW voltage	I _{ERROL} = 25 mA; V _{DD} = 1.7 V	-	-	0.5	V
I _I	Input current	All inputs, V _I = V _{DD} or GND; V _{DD} = 1.9 V	-	-	±5	μA
I _{DD}	Static standby current	$\overline{\text{RESET}}$ = GND; V _{DD} = 1.9 V	-	-	200	μA
	Static operating current	$\overline{\text{RESET}}$ = V _{DD} ; V _{DD} = 1.9 V; V _I = V _{IH(AC)} or V _{IL(AC)}	-	-	80	mA
I _{DDD}	Dynamic operating current — clock only	$\overline{\text{RESET}}$ = V _{DD} ; V _I = V _{IH(AC)} or V _{IL(AC)} ; CK and $\overline{\text{CK}}$ switching at 50% duty cycle. I _O = 0; V _{DD} = 1.8 V	-	†	-	μA/MHz
	Dynamic operating current — per each data input	$\overline{\text{RESET}}$ = V _{DD} ; V _I = V _{IH(AC)} or V _{IL(AC)} ; CK and $\overline{\text{CK}}$ switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. I _O = 0; V _{DD} = 1.8 V	-	†	-	μA/MHz
Input capacitance values, SSTUA32S865 single die version						
C _i	Input capacitance, Data inputs	V _I = V _{REF} ± 250 mV; V _{DD} = 1.8 V	2.5	-	3.5	pF
	Input capacitance, CK and $\overline{\text{CK}}$	V _{ICR} = 0.9 V; V _{ID} = 600 mV; V _{DD} = 1.8 V	2	-	3	pF
	Input capacitance, $\overline{\text{RESET}}$	V _I = V _{DD} or GND; V _{DD} = 1.8 V	†	-	†	pF
Input capacitance values, SSTUA32D865 dual die version						
C _i	Input capacitance, Dn, PARIN	V _I = V _{REF} ± 250 mV; V _{DD} = 1.8 V	2.5	-	3.5	pF
	Input capacitance, $\overline{\text{DCS}}_{\text{n}}$	V _I = V _{REF} ± 250 mV; V _{DD} = 1.8 V	4	-	6	pF
	Input capacitance, CK and $\overline{\text{CK}}$	V _{ICR} = 0.9 V; V _{ID} = 600 mV; V _{DD} = 1.8 V	4	-	6	pF
	Input capacitance, $\overline{\text{RESET}}$, CSGateENable	V _I = V _{DD} or GND; V _{DD} = 1.8 V	†	-	†	pF

† The vendor must supply this value for full device description.

2.12 Timing requirements

Table 7 — Timing requirements over recommended operating free-air temperature range (see Figure 6)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clock}	Clock frequency		-	410	MHz
t_W	Pulse duration, CK, $\overline{\text{CK}}$ HIGH or LOW		1	-	ns
t_{ACT}	Differential inputs active time	(See Notes 1 and 2)	-	10	ns
t_{INACT}	Differential inputs inactive time	(See Notes 1 and 3)	-	15	ns
t_{SU}	Setup time, Chip Select	Chip select valid before clock switching	0.7	-	ns
	Setup time, Data	D[n] valid before clock switching	0.5	-	ns
	Setup time, PARIN	PARIN before CK and $\overline{\text{CK}}$	0.5	-	ns
t_{H}	Hold time	Input to remain valid after clock switching	0.5	-	ns
	Hold time, PARIN	PARIN after CK and $\overline{\text{CK}}$	0.5	-	ns

NOTE 1 This parameter is not necessarily production tested.

NOTE 2 Data inputs must be active below a minimum time of t_{ACT} (max) after $\overline{\text{RESET}}$ is taken HIGH.

NOTE 3 Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} (max) after $\overline{\text{RESET}}$ is taken LOW.

2.13 AC specifications

Table 8 — Switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see section 3.1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MAX}	Maximum input clock frequency		410	-	MHz
t_{PDM}	Propagation delay	Clock to output (see Note 1)	1.25	1.90	ns
t_{LH}	LOW-to-HIGH delay	CK and $\overline{\text{CK}}$ to $\overline{\text{PTYERR}}$	1.2	3	ns
t_{HL}	HIGH-to-LOW delay	CK and $\overline{\text{CK}}$ to $\overline{\text{PTYERR}}$	1	3	ns
t_{PLH}	LOW-to-HIGH propagation delay	from $\overline{\text{RESET}}$ to $\overline{\text{PTYERR}}$	-	3	ns
t_{PDMSS}	Propagation delay, simultaneous switching	Clock to output (See Notes 1 and 2)	-	2.00	ns
t_{PHL}	Propagation delay	Reset to output	-	3	ns

NOTE 1 Includes 350 ps of test-load transmission line delay.

NOTE 2 This parameter is not necessarily production tested.

2 Device standard (cont'd)
2.14 Output buffer characteristics

Table 9 — Output edge rates over recommended operating free-air temperature range
(see section 3.2)

Symbol	Parameter	Conditions	Min	Max	Unit
dV/dt _r	rising edge slew rate		1	4	V/ns
dV/dt _f	falling edge slew rate		1	4	V/ns
dV/dt _Δ [†]	absolute difference between dV/dt _r and dV/dt _f		-	1	V/ns

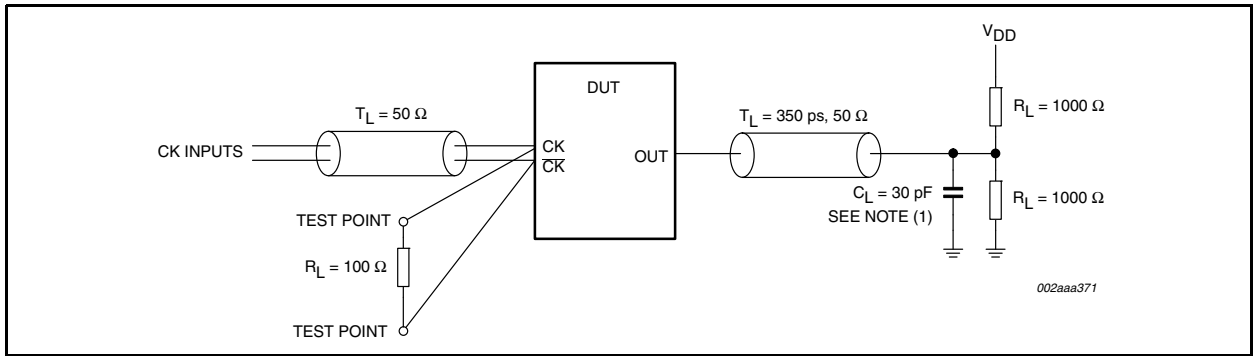
[†] Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

3 Test circuits and switching waveforms

3.1 Parameter measurement information (V_{DD} = 1.8 V ± 0.1 V)

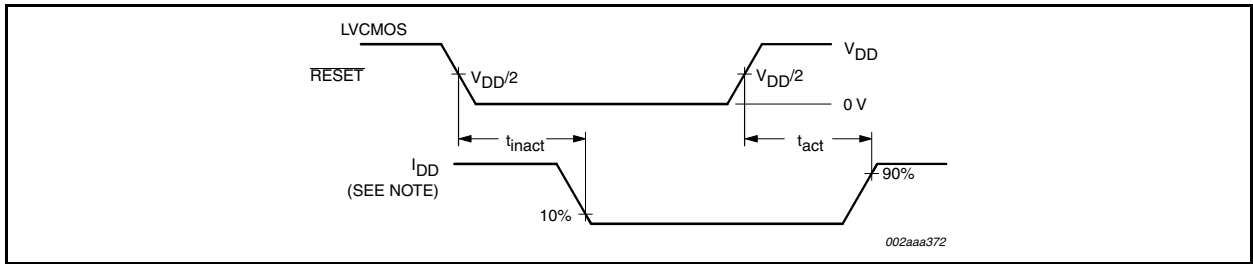
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz;
Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



(1) C_L includes probe and jig capacitance.

Figure 10 — Load circuit

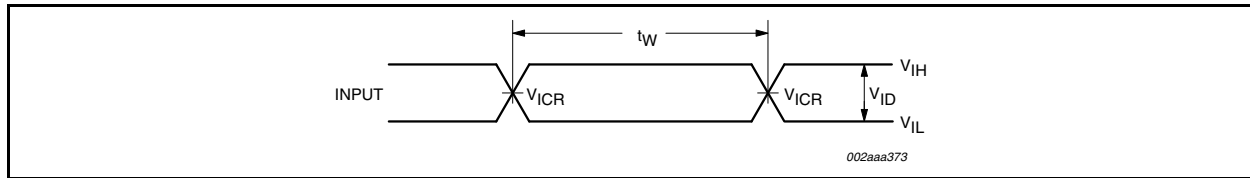


I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Figure 11 — Voltage and current waveforms; inputs active and inactive times

3 Test circuits and switching waveforms (cont'd)

3.1 Parameter measurement information (cont'd)

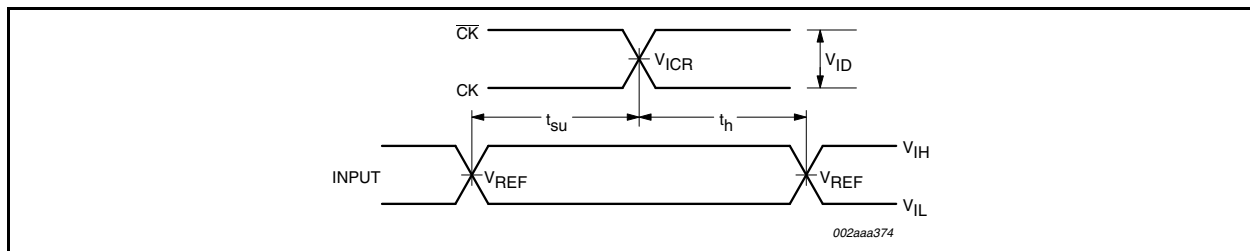


$V_{ID} = 600 \text{ mV}$

$V_{IH} = V_{REF} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

$V_{IL} = V_{REF} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 12 — Voltage waveforms; pulse duration



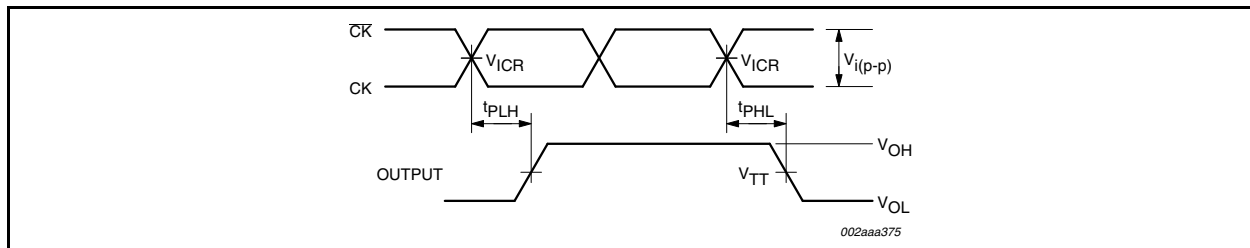
$V_{ID} = 600 \text{ mV}$

$V_{REF} = V_{DD}/2$

$V_{IH} = V_{REF} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

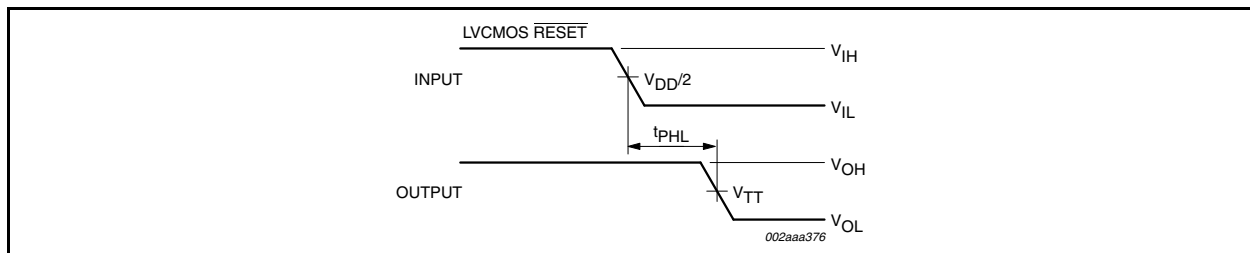
$V_{IL} = V_{REF} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 13 — Voltage waveforms; set-up and hold times



t_{PLH} and t_{PHL} are the same as t_{PD} .

Figure 14 — Voltage waveforms; propagation delay times



t_{PLH} and t_{PHL} are the same as t_{PD} .

$V_{IH} = V_{REF} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

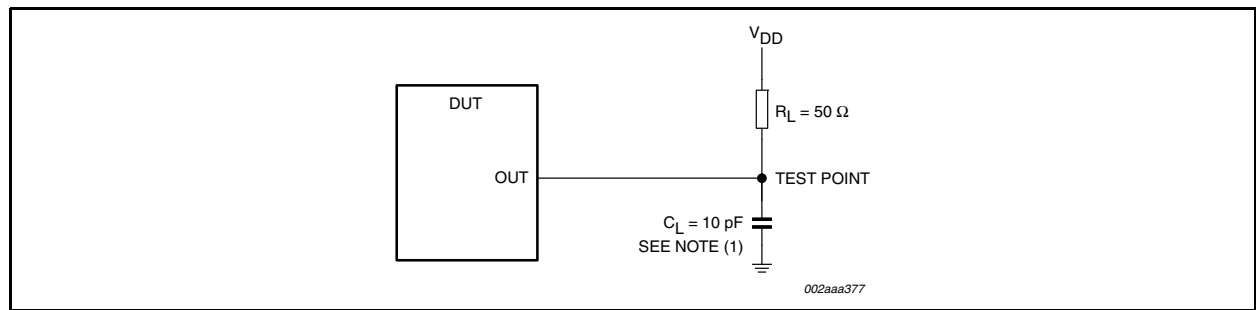
$V_{IL} = V_{REF} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 15 — Voltage waveforms; propagation delay times

3 Test circuits and switching waveforms (cont'd)

3.2 Output slew rate measurement information ($V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$)

All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$; $Z_o = 50\ \Omega$; input slew rate = $1\text{ V/ns} \pm 20\%$, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 16 — Load circuit, HIGH-to-LOW slew measurement

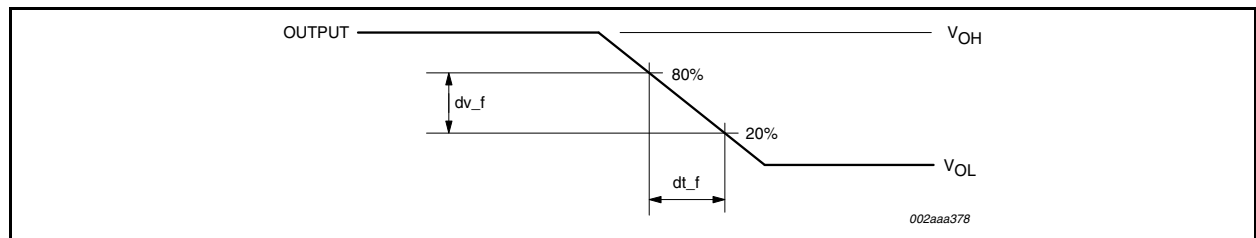
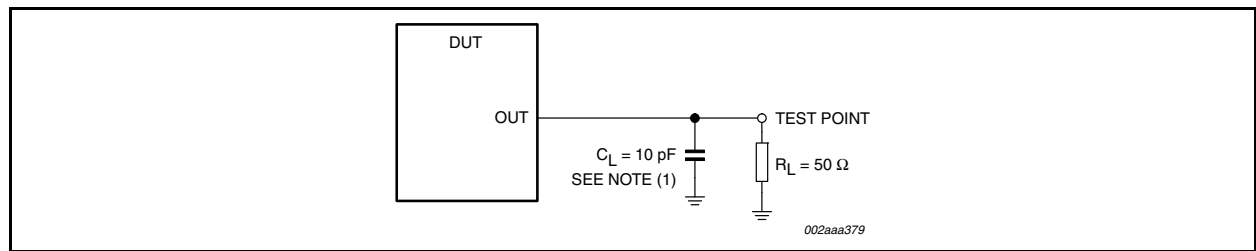


Figure 17 — Voltage waveforms, HIGH-to-LOW slew rate measurement



(1) C_L includes probe and jig capacitance.

Figure 18 — Load circuit, LOW-to-HIGH slew measurement

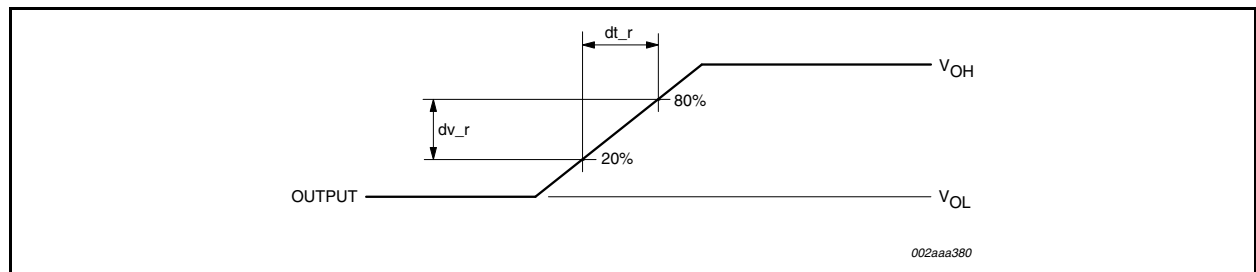
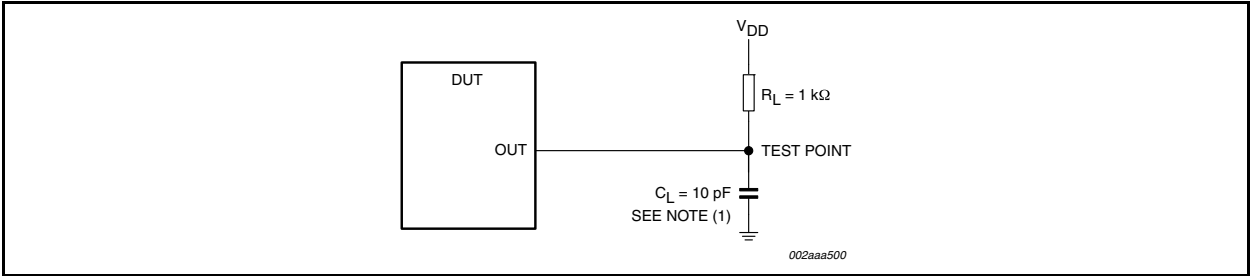


Figure 19 — Voltage waveforms, LOW-to-HIGH slew rate measurement

3 Test circuits and switching waveforms (cont'd)

3.3 Error output load circuit and voltage measurement information ($V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$)

All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$; $Z_o = 50\ \Omega$; input slew rate = $1\text{ V/ns} \pm 20\%$, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 20 — Load circuit, error output measurements

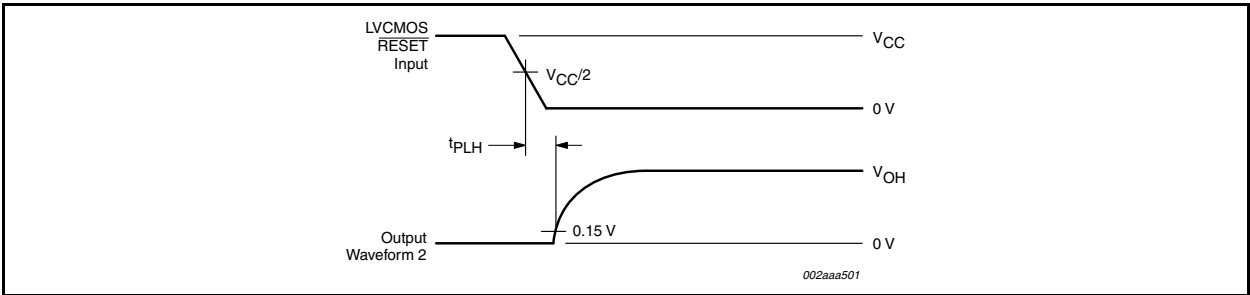


Figure 21 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to RESET input

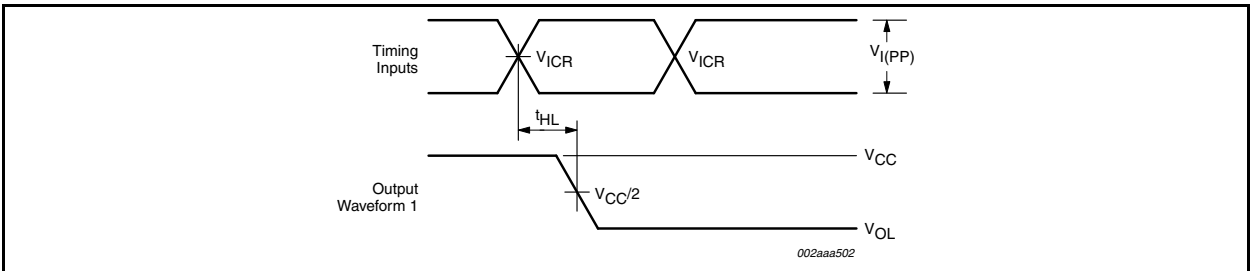


Figure 22 — Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs

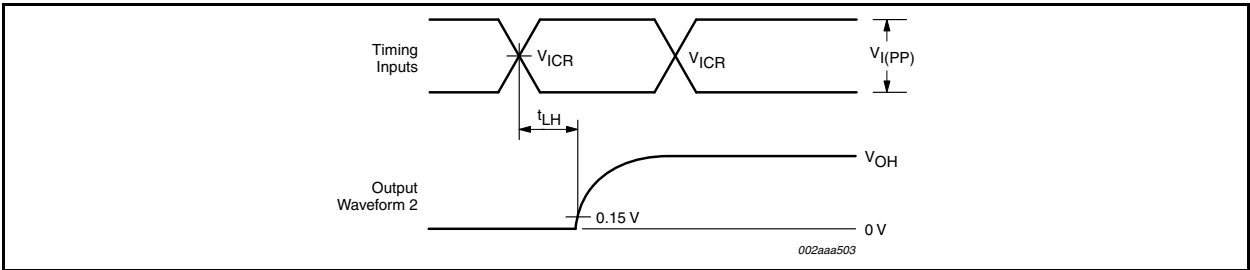


Figure 23 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs

4 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*

JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*

JESD8-7, *1.8V +/- 0.15V (Normal Range), and 1.2 - 1.95V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits.*

JESD8-15, *Stub Series Terminated Logic for 1.8 V (SSTL_18).*

JESD21-C, *Configuration for Solid State Memories.*

JESD82-7A, *Definition of the SSTU32864 1.8 V Configurable Registered Buffer for DDR2 RDIMM Applications*

JESD82-9A, *Definition of the SSTU32865 1.8 V Registered Buffer with Parity for DDR2 RDIMM Applications*

Annex A (informative) Differences between JESD82-19A.01 and JESD82-19A

This table briefly describes most of the changes made to entries that appear in this standard, JESD82-19A.01, compared to its predecessor, JESD82-19A (May 2007). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Date	Person	Location	Change
2021-06-03	B. Gervasi	Table 1	Changed master to controller

A.1 Differences between JESD82-19A and JESD82-19 (May 2006)**Page Description of change**

This information not available at time of publication.



Standard Improvement Form

JEDEC JESD82-19

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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3. Other suggestions for document improvement:

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